PULSUS Journal of
Material Engineering & Applications
Abstract

Gate-all-around Si nanowire FET with low-thermal-budget process for monolithic three-dimensional integrated circuits

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Abstract:
For 3D monolithic integrated (3DMI) technology, the most important task is to fabricate high performance stackable device and prevent damage on underlying device and structure during processes. In this article, we propose a green nanosecond laser crystallization and laser spike anneal process to fabricate 3D stackable ultra-thin body transistors and realize a sequentially layered integrated circuit. As identified, the possible failure mechanism of underlying device using laser process is the directly penetrated laser light and the heat from the high temperature surface. By optimizing the process conditions and stacking layer thickness, we can reduce the thickness of interlayer dielectric to about 200-nm-thin which quite reducing the delay and power loss from interconnects for 3DIC.

Biography:
Tung-Ying Hsieh has his expertise in monolithic 3DIC. He used to be an engineer in TSMC. And vising in Stanford University to conduct AI chips experiment. Now he is pursuing his PhD in Electronics engineering, NTHU, Hsinchu, Taiwan.

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28th International Conference on Materials Research and Technology; June 22-23, 2020; Osaka, Japan.

Citation: Tung-Ying Hsieh, Gate-all-around Si nanowire FET with low-thermal-budget process for monolithic three-dimensional integrated circuits; Materials Technology and Research 2020; July 22, 2020; Osaka, Japan.